Study of resistance changes impact on power of resistive-load inverter by using 90nm and 65nm technologies

Forough Fallahi and Dr Mahmood Aleshams
Student of MA degree, Islamic azad university,fasa branch
Member of Islamic azad university faculty,fasa branch
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Name of the Presenter: Forough Fallahi

Abstract

With the increasing development of science and technology in today's world, Electronic chips go into nanotechnology. logical complexity is exponential growth in chip . Advances in integrated circuits manufacturing technology are posing particular size reduction. On the other hand, power is one of the most important factors that will be evaluated in an electronic circuit. This paper has tried to study of resistance changes impact on the Dc and dynamic power of resistive-load inverter circuit by using nanotechnologies. And the distribution of these powers can be applied in.

Key words: Reduce of power, Resistance, Hspice software, resistive-load inverter.

1. Introduction

VLSI or Very Large Scale Integration, An area dense with electronic components is very small deals in the area. The circuits are located on the surface of a few square millimeters. This is a great opportunity to do the work that has provided so far is not possible. Integrated circuits have been for a long time. But the super fast growth of the technology and its capabilities is to expand its application in life. Looking to see Moore's law which in terms of computing power IC power, performance, area, fertility and so have an exponential growth and the combined effect of these benefits is that man can now include IC circuits in their requirements.

Inverter is one of the important logical gates; does NOT logical function on the input variable. Therefore, the design basis for the design of digital circuits is considered inverter. In MOS inverter circuits, both the A and B input variable node voltages with respect to ground potential are shown. Using positive logic, a Boolean value, the voltage VDD and VSS voltage or ground zero boolean show.

2. electrical characteristics of resistive-load inverter

As shown in Fig. 1; this inverter has an increase-nMOS transistor as a driver and a resistance as a load.

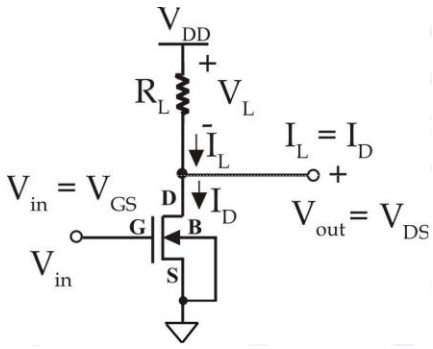

Fig 1. Inverter with resistance load (resistive-load inverter)

As a practical estimate of the area the transistor channel MOS, we use the W * L. Thus, for each MOS transistor has a minimum when both the gate area (channels) to the extent that the limits of technology allows small to be selected, However, this may require other design criteria such as noise margin, output current drive capability and switching speed is dynamic contrasts**.**Circuit operation of Fig. 1 is; if the input voltage of the transistor smaller then threshold voltage VTH, the transistor is in the off state. Once the input voltage is greater than VTH, driver transistor starts to conduct and the beginning of the MOSFET is in the saturation region. By increasing the input voltage, current of driver increase and output voltage Vout will start to drop. Finally, transistor is in the linear region and the output voltage of the transistor into the sanctity linear increase in the input transistors stay in the linear region, is reduced.

3. power and viewpoint of reduce of power

A. DC power

Inverter circuit DC power can be multiplied by supply voltage and the amount of current drawn from the power supply in stable case. Static power is calculated from the following formula:

$$P_{DC}=V_{DD}.\ I_{DC} \tag{1}$$

Dc current that is drawn by the circuit inverter may be highly dependent on the input and output voltages. Suppose the input voltage level corresponding to 50% of the time, the logic zero and the remaining 50% is associated with logic. The total DC power circuit can be estimated from the following formula**:**

$$P_{DC}=V_{DD}/2.\ [\ I_{DC}\ (\text{Vin=LOW})\ +I_{DC}\ (\text{Vin=High})\ ] \tag{2}$$

B. Dynamic power

The total dynamic power is obtained by the following formula:

$$P_{dyn}=C_L.V_{DD}^{2}.f.\ \alpha+\ (V_{DD}^{2}/2R) \tag{3}$$

According to the Eq. 3, Pdyn with capacitance CL, the square of the supply voltage Vdd, α Switching activity, clock frequency f and resistance R, is proportional. [4]
Consequently, reducing power consumption can be achieved by the following factors**:**
•reduced output capacitance, CL

- reducing the supply voltage, Vdd
- reduction the Switching activity, α
- reducing the clock frequency, f
- increasing the resistance, R

Dynamic power dissipation due to charge and discharge the parasitic capacitors in circuit. To calculate the dynamic power dissipation with a capacitive load CL stimulated an inverter we use**.**This part of the paper, a very important role of power in the reduce the inverter is described and explained how it is important in a circuit inverter. The use of nanotechnology in the manufacture of electronic chips, such as transistors while reducing its dimensions (length and width) is; the area will also be naturally reduced. Reducing the area of the transistor is considered less current draw of the circuit, the less power it consumes. This reduction is such that the lower limit of the nanotechnology move forward, we will further decrease**.**But there is something that, when we talk about the size of a few tens of nanometers in dealing with a limited number of atoms.Silicon atoms as the basic element in the construction of modern electronic circuits, 0.2 nm; If we consider the distance between the atomic bonds, We see that the proposed dimensions For length of the channel, as we face the difficult task ahead of us with a few dozen atoms. Another issue is the size of the transistor manufacturing technology in nanoscale transistor construction costs and simultaneously having high resolution and the volume is also limited**.**

According to the description given in the text, in this paper, we use 90 nm and 65 nm technologies for increase-Nmos transistors in circuit, then we can calculate both of the dynamic and DC power by various amounts of resistance has been studied in the tables**.**

4. power of resistive-load inverter

For calculate power of resistive-load inverter; we consider two cases **:**

A). Vin = 0; in this case Nmos transistor is cut off**.**

$$IL=ID=0\rightarrow P\ (Vin=0)=0 \quad (4)$$

B). (Vout = V_{OL}) Vin = V_{DD}; in this case driver and load transistors, guides non-zero current**.**

$$I_{DC}(Vin='1')=I_L=I_D=(V_{DD}-V_{OL})/R_L \quad (5)$$

According to Eqs. 4~5 the total power of resistive-load inverter is obtained as follows**:**

$$P_{DC}=P(Vin='1')=(V_{DD}/2).[(V_{DD}-V_{OL})/R_L] \quad (6)$$

5. Results and Tables

Circuit simulation of Fig. 1 is performed using Hspice software. Input is a pulse voltage source and paramerers of increase-Nmos transistor for 90nm and 65nm are specified in the following:

90nm: L = 0.08 u W = 0.12 u
65nm: L = 0.06 u W = 0.12 u

Profile parameters in order to determine the change of resistance in the circuit:

Supply voltage: 3.3v, 1.3v, 0.5v
Resistance: 0.01, 600, 1k, 600k
Capacitors: 100fF

R ; V_{DD}	3.3v	1.3v	0.5v
0.01	1.34501m	82.15141u	415.8211n
600	1.26051m	80.65141u	415.3711n
1k	1.22201m	79.60141u	415.0211n
600k	9.07325u	1.402908u	190.5709n

Table 1. Check the DC power for different values of resistance and supply voltage in 90 nm

R ; V_{DD}	3.3v	1.3v	0.5v
0.01	350.1002u	22.75001u	6.31538n
600	347.4502u	22.65001u	6.31527n
1k	345.7002u	22.58001u	6.31501n
600k	9.02527u	1.38951u	6.12027n

Table 2. Check the DC power for different values of resistance and supply voltage in 65 nm

6. Conclusions

According to Eq. (6) and Tables 1~2 in a particular technology (such as 90nm or 65nm), the increase in resistance for a particular supply voltage (eg 3.3V);power can be reduced. Furthermore, by reducing the supply voltage (eg 0.5V vs. 3.3V) for a specific resistance (eg 1kh); power can be reduced**.**

Note that in this case there is a quadratic dependence with respect to the power supply voltage, at each step of the dynamic power can be further reduction DC**.**

The investigation has determined that the changes in resistance can both DC and dynamic scattering effects are significant**.**

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