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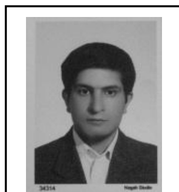
A Method for Determining the Critical Parts of Electronic Circuits into EFT/B



B.Gh. Family, V.H. Vaghef, and M.Shabro
Communication Department, Niroo Research Institute, Iran.
(behnam_gh_f@yahoo.com, vvaghef@nri.ac.ir, mshabro@nri.ac.ir)

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Name of the Presenter: Vahid Hamiyati Vaghef

Abstract

Electrical Fast Transient/Burst Immunity testing is an important safety measure that examines the disturbances caused by switching power supplies, inductors, contact relays, or high voltage switches on electric and electronic equipment and allows system designers to study the efficiency of the equipment under this type of system disturbance. If a compliancy test is performed according to the current standard method of testing and the result shows a failure, detecting the susceptible point is difficult, and repeating the test in the EMC reference laboratory is very time consuming and costly. With a low-cost EFT/B simulator circuit, the critical and sensitive points can be identified sooner and they can be resolved at design phase.

Key words: Electromagnetic Compatibility, EFT/B.

1. Introduction

Nowadays, various electronic equipments are used in the vicinity of each other. The electromagnetic compatibility between them and environment is very important, especially in industrial environments.

The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment is Electromagnetic Compatibility (EMC), and immunity is the ability of a device, equipment or system to work without performance degradation in the presence of an electromagnetic disturbance. Electrical Fast Transient/ Burst (EFT/B) Immunity Testing is one means of measuring such immunity, as described in IEC 61000-4-4 (2012).

For designing industrial devices, considering guidelines in hardware and software components is essential. EMI reduction and EMC improvement will be achieved by using protection devices such as shields, grounding, filters, isolators, chocks, ferrite beads, varistors, transient voltage suppressors (TVS), and also appropriate PCB layout design. Typical EFT/B failures are due to an inadequate or unavailable interface ground reference. Therefore, designers should try to use appropriate ground reference and protection at the incoming or outgoing ports. In addition, due to the software layer in most systems, electromagnetic immunity

should be considered in software. Software problems include data loss, system malfunction, or an otherwise impairment of the process. Software can be designed to find and correct errors before they become dangerous, by reading critical inputs several times; checking data, counters, and pointers validity; and using serial protocols, watchdog timers, and so on.
In general, resolving the problems caused by the presence of several kV pulses is a sophisticated process. Theoretical considerations of immunity against disturbances and radiation are effective, but insufficient. Despite an electronic device's seemingly complete design, sensitive parts of the circuit against EFT/B may still exist and performing standard tests on the entire system may not exactly identify the sensitive parts of the circuit. These sensitive parts may lead the system to fail an immunity test. However, Inspecting the susceptible points is difficult in general, and it requires several trial and error tests which are very time consuming and costly. Designers need low-cost and non-destructive tests to successfully transition from their model designs to finished industrial designs. Thus, the use of simulations during the system and board design phases is recommended for extracting the critical points.
This article presents a simple and inexpensive way for determination of critical points respect to the EFT/B pulses, as a preliminary evaluation of the system.

2. Characteristics of Electrical Fast Transient/ Burst

The EFT/B test aims to simulate the disturbances created by a 'showering arc' at the contacts of an ordinary AC mains switch or relay contacts as it opens. This test evaluates the immunity of electrical and electronic equipment when subjected to EFT/B on supply, signal, control and earth ports. This phenomenon is modeled as Fig. 1. The characteristic of burst generator, test setup, test verification, and test procedure are described in IEC 61000-4-4 standard. It has fast rise time, low energy, high voltage, and consists of a single unidirectional impulse repeated at a 5kHz(100kHz) in bursts lasting 15(0.75) milliseconds each, with three bursts per second. Different voltage test levels are defined in standard as Table 1. The test severity level and frequency are selected according the equipment installation environment.

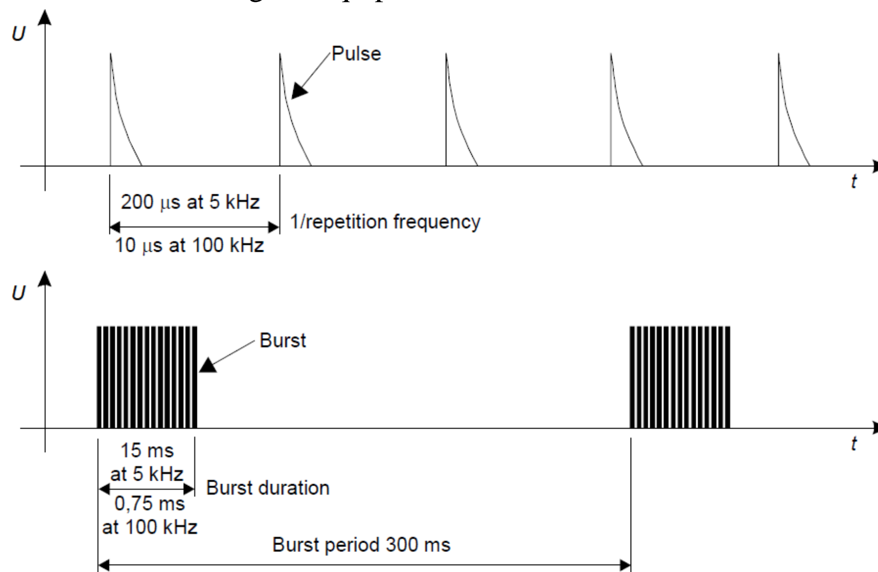

Fig 1: Representation of an EFT/B according to IEC 61000-4-4.

Level	Power ports, earth port (PE)		Signal and control ports	
	Voltage peak kV	Repetition frequency kHz	Voltage peak kV	Repetition frequency kHz
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	special	special	special	special
The use of 5kHz repetition frequency is traditional; however, 100kHz is closer to reality. Product committees should determine which frequencies are relevant for specific products or product types.				
"X" can be any level, above, below or in between the others. The level shall be is in specified in the dedicated equipment specification.				

Table 1. Test voltage and repetition frequency of the impulses according to IEC 61000-4-4.

3. Design and Implementation of Low-Cost EFT/B Generator

The simplified circuit diagram of the EFT/B generator is given in Fig. 2. In this circuit, a high voltage source charges a Cc capacitor and the charging and discharging of capacitors is controlled by a Switch. The desired pattern is produced, as shown in Fig. 1.

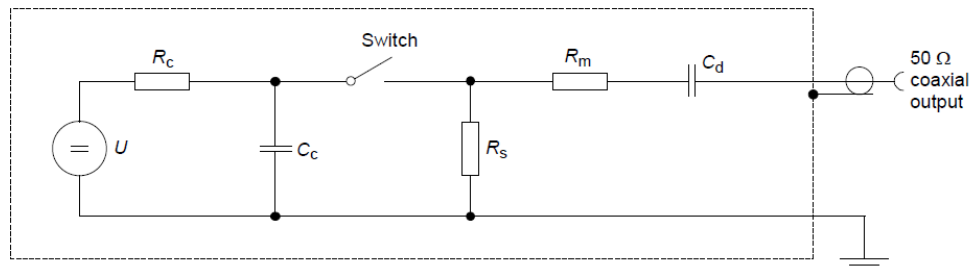

Fig 2: Simplified circuit diagram of an EFT/B according to IEC 61000-4-4.

The purpose of this study is to explain the design and implementation of a simulator for EFT pulse generation in order to determine the critical points of electronic circuits. A block diagram of the designed circuit that simulated EFT/B generator is shown in Fig. 3.

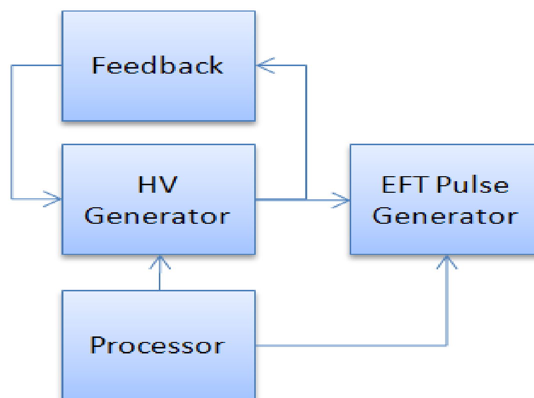

Fig 3: Block diagram of the designed EFT/B generator

As mentioned before, a high voltage circuit is required to produce EFT pulses. Since these pulses have high voltage with low energy, the low-cost circuit in Fig. 4 is proposed to meet the requirements. The output voltage of this circuit is simulated by HSPICE software as shown in Fig. 5. This graph shows the voltage across the C1 capacitor. This circuit produces voltages higher than 400 V in less than 50ms. The main advantage of this circuit is its ability to generate high voltages using a voltage of 12 V. This makes the circuit to be portable. The power consumption of the circuit is also significantly low. The portability of this circuit allows users to test different parts of a large system easily.

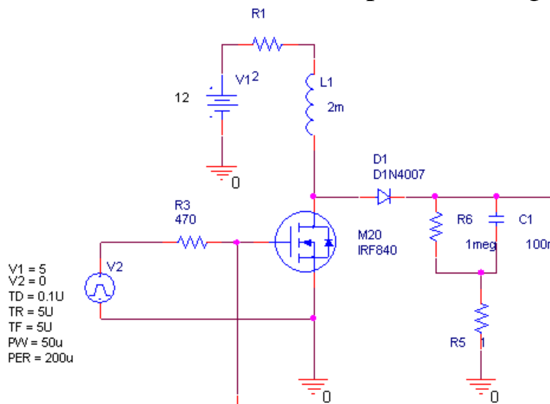

Fig 4: High voltage generator circuit.

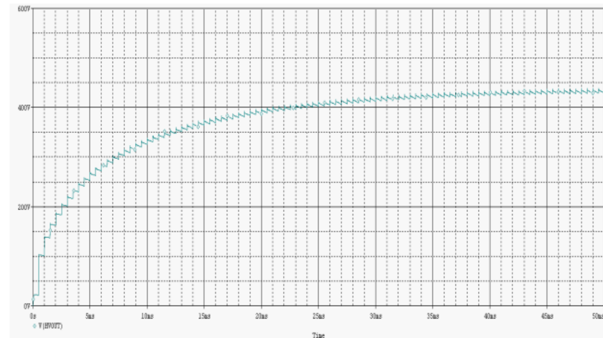

Fig 5: Output voltage of Fig 4.

To generate higher voltages, MOSFET transistors with higher breakdown voltages can be used. For example: FS10SM (with 800V breakdown) or IXZR08N120B (with 1200V breakdown) are good instances.

Circuit's load changes alter the output voltage which is controlled by sampling the output voltage and adapting the input frequency. However, using this method is not recommended because the efficiency of the circuit decreases. The feedback circuit shown in Fig. 6 can control the output voltage without decreasing its efficiency.

With the feedback circuit, the output voltage will vary with changes in the input pulse shape and prevent excessive output voltage. The level of output voltage is determined by R14, R15 and the Zener diode D2. The circuit output has different voltage levels by using Zener diodes with different breakdown voltages.

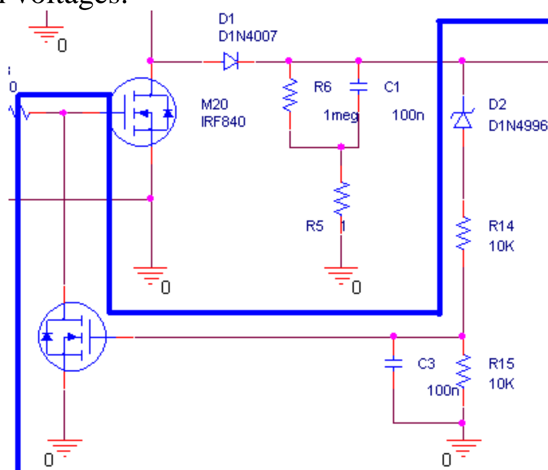

Fig 6: Feedback for voltage control.

By using a simple circuit similar to Fig. 7, EFT pulses can be generated. The transistor pulsed on and off simultaneously with input pulses and discharges of high voltage stored in the C2 capacitor in the minimum possible time. The output of the circuit is shown in Fig. 8. This output can be applied to the circuit under testing by using another capacitor.
The output pulses generated by this circuit are not fully compatible to the pulses described in the standard IEC61000-4-4 because of the capacitor's internal series resistance and the transistor's on delay time. But they can reveal the sensitive parts of the circuit under testing to standard EFT pulses.

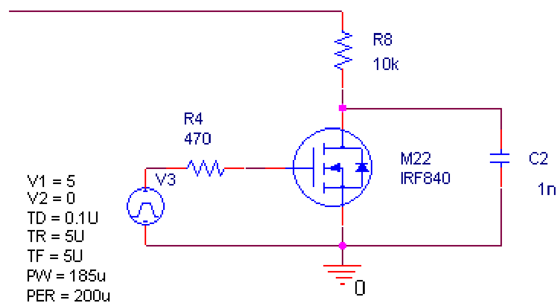

Fig 7: EFT pulse generator circuit.

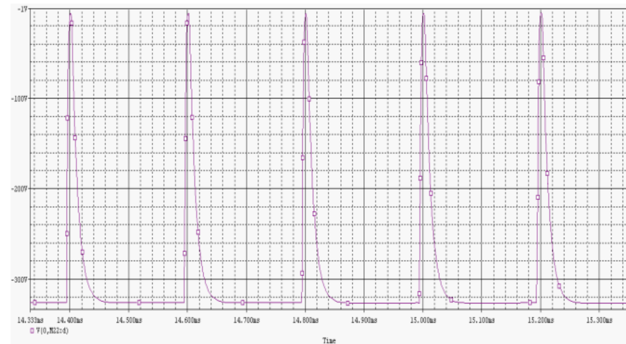

Fig 8: EFT pulses of Fig 7.

It is also possible to use avalanche transistors connected in series and operated close to their avalanche breakdown as shown in Fig. 9 for switching very high voltage pulses. For example, a ZTX415 transistor is suitable for this purpose.

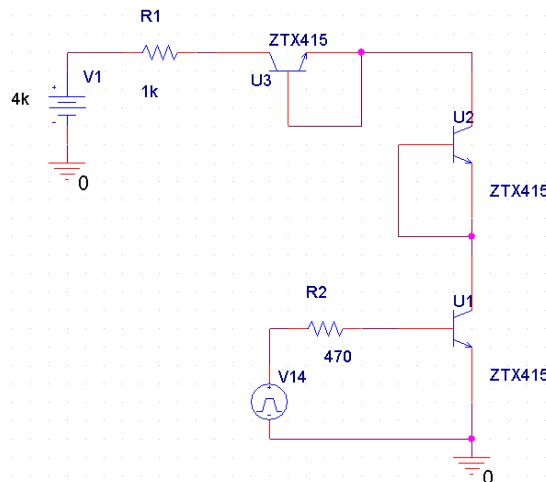

Fig 9: Use of avalanche transistors connected in series.

In order to generate the input pulse for switching a MOSFET transistor, a microcontroller is used. The microcontroller output pin must be isolated from a high voltage generator; otherwise the distortion produced by this circuit prevents the proper operation of the microcontroller. Figs. 10~11 show the schematic and board of the designed circuit and the EFT pulses generated by this simulator are shown in Figs. 12~13 that measured by HM2008 2Gsa HAMEG oscilloscope. The impulses are repeated at 5kHz in bursts lasting 15ms each, and the period of bursts is set to 300ms.

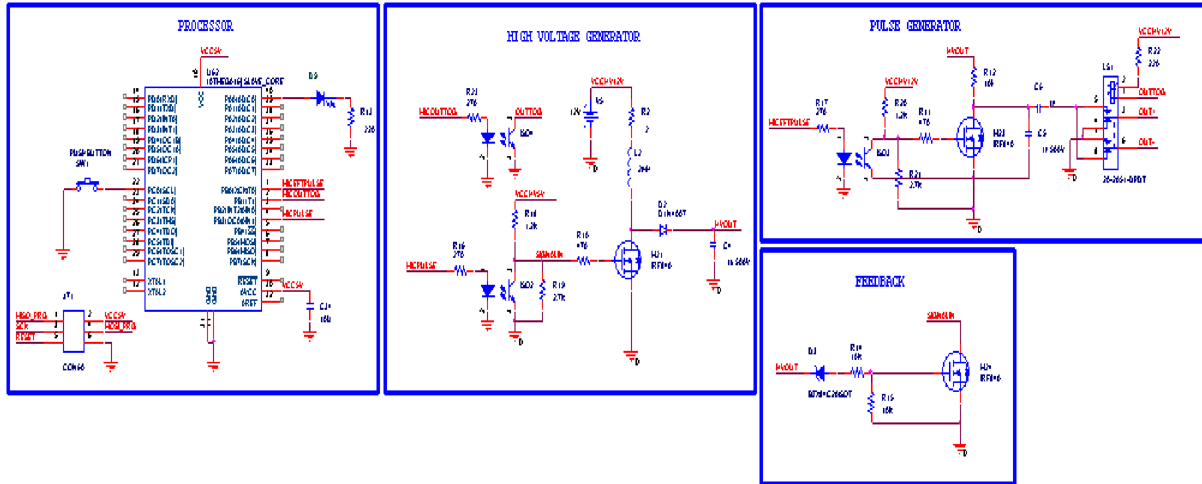

Fig 10: Schematic of designed EFT simulator circuit.

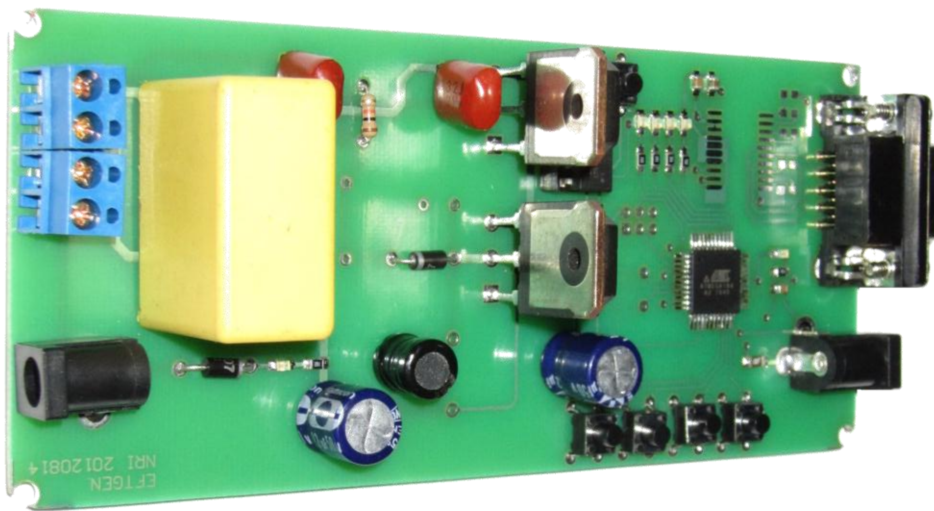

Fig 11: Designed EFT generator board.

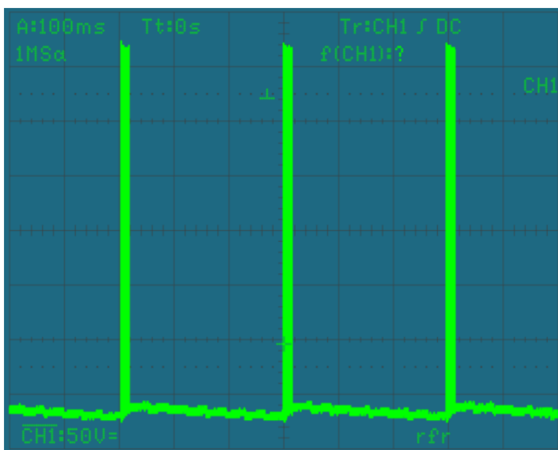

Fig 12: EFT pulses generated by simulator.

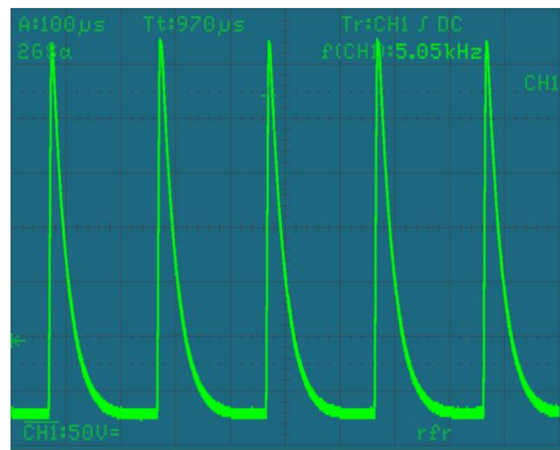

Fig 13: Waveform of a single pulse.

According to IEC 61000-4-4 the EFT pulse is applied with a coupling network to the power ports and with a coupling clamp to input/output cables of the EUT. Due to the use of protective components in these ports, the amount of EFT/B pulses energy will decrease. Therefore, if the output of the designed circuit with lower voltage than the standard EFT/B pulses is applied to the internal nodes of the circuit under testing, it is similar that a standard EFT/B pulses has been applied to the entire system and it is possible to identify the sensitive parts of the circuit under testing by this method. As mentioned previously, because of the low energy of the EFT/B generator pulses, its output can be directly applied to all the components on the circuit during its normal function and the circuit behavior can be evaluated.

4. Conclusions

Developments of EFT/B simulator circuit for the design and certification of complex systems outcome:

- Product design cost reduction
- Time and cost reduction in the certification process
- System Investigating for standard development

This simple and low-cost circuit can be used in the design phase of any electronic circuits to evaluate their immunity against EFT/B.

The results of using this method to find the critical points of a DTPS-8C (a Digital Teleprotection System) against EFT/B pulses, confirmed the efficiency and non-destructive nature of this approach.

Acknowledgements

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